Effect of Annealing on Structural and Electrical Properties of Epitaxial Silicon Emitters Produced by Low Temperature PECVD

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Standard P-N junctions are usually obtained by diffusion of dopants on the c-Si wafer. Renewed interest for crystalline silicon growth of emitters by epitaxy is developing in the photovoltaic community. One of the investigated techniques, atmospheric pressure chemical vapor deposition (CVD), has already shown its potential with a 22.5% n-PERT solar cell[1]. This technique can be used for either absorber or emitter formation but in both cases the process temperatures exceed 900°C. Another approach, which is studied here, is to deposit doped epitaxial silicon (epi-Si) layers by plasma-enhanced CVD (PECVD) at temperatures below 400°C. The advantages of such a method are the lower thermal budget, the better control of the doping profile compared to diffusion and the possible cost reduction. In this work, we focus on the effect of annealing on the structural and electrical properties of doped epi-Si layers in order to assess the quality of the P-N junction, as it is critical for reaching high conversion efficiencies. A FZ n-type <100> silicon wafer was chosen as substrate and the epitaxy was performed in a SiH_4/H_2/TMB gas mixture at 175°C. The deposition temperature was determined based on previous results using the same chemistry where a 15,4% cell was achieved[2]. However, in the as-deposited state our samples have poor performances. Indeed, an annealing step is needed to activate the dopants. Sheet resistance and conductivity measurements of the epi-Si films indicate a significant gain in conductivity with increasing annealing temperature. Exodiffusion reveals the probable correlation between the amount of hydrogen present in the layer and the activation. Furthermore, X-ray diffraction measurements show the evolution of the lattice parameter of the epi-Si films depending on the annealing temperature.

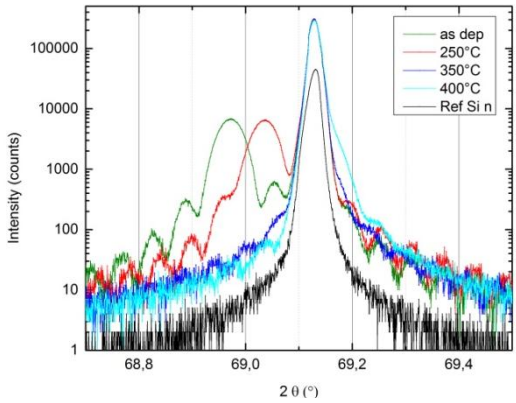

Figure 1 : XRD ω/2θ scan for (004) planes of epi-Si layers after annealing at different temperatures

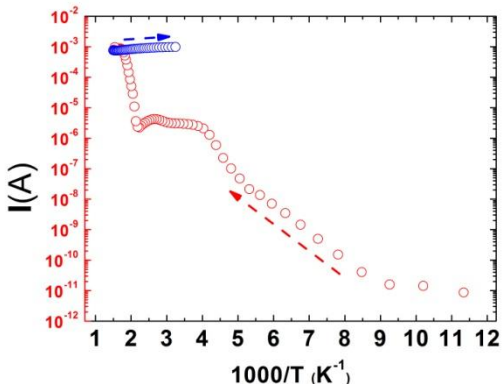

Figure 2 : Measurement of current, proportional to conductivity, as a function of temperature

1. Kuzma-Filipek, I. *et al.* Simplified cleaning for 22.5% nPERT solar cells with rear epitaxial emitters. *Sol. Energy Mater. Sol. Cells* **158,** 19–23 (2016).
2. Labrune, M. Silicon surface passivation and epitaxial growth on c-Si by low temperature plasma processes for high efficiency solar cells. (2011).