GaAs and GaAsP nanowire solar cells grown on patterned Si substrates by MBE: recent results and perspectives

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Nanowire (NW) solar cells have emerged recently as a possible route to effectively implement III-V on Si tandem devices. NW-based devices have the potential to eliminate lattice and thermal mismatch constraints, to efficiently trap light with minimal amount of material and to implement novel device concepts such as hot-carrier solar cells. The optimum bandgap for a top cell in a dual-junction tandem with Silicon as the bottom cell has been calculated to be 1.7 eV [1], which is in the range of III-V alloys like InGaP and GaAsP. Despite its bandgap being lower than the optimum, GaAs remains a material of interest because of the high quality achievable with many growth techniques. It also provides a reliable base to test the nanowire architecture without the complication of ternary alloy epitaxy. Moreover, its material properties are well known and could be readily used for characterization and modelling, even in nanowire geometry. Record single-junction nanowire devices have been recently reported for GaAs [2].

We present our most recent results on the growth of GaAs(P) nanowire arrays by MBE on patterned Si substrates (figure a), highlighting some critical constraints in the design and epitaxy of nanowire solar cells. The choice of patterned substrates derives from the necessity of a uniform ensemble of nanowires to have a good control on the junction structure, namely doping levels and thickness of the different active layers.

The following points will be particularly addressed and discussed:

- Different strategies lead to high yield of vertical GaAsP nanowires, from 85% (GaAs) to 99% (GaP). The effects of growth velocity and alloy composition are found to be critical parameters.
- Be-doped GaAs NW cores with p-type doping in the $10^{19}cm^{-3}$ range were grown (figure b).
- Si-doped GaAs NW shells with n-type doping of $10^{18}cm^{-3}$ were achieved. The strong effect of growth temperature on polarity and self-compensation of Si-doped nanowire shells, as well as the incorporation mechanisms on different crystal facets will be described.
- Long segments (> 1µm) of zinc blende GaAs nanowires without any stacking fault were obtained.
- The cathodoluminescence mapping allowed a quantitative assessment of the n-type and p-type doping levels (figure c) in single nanowires [3].

Finally, by merging all these building blocks, nanowire single-junction devices were grown, fabricated and tested. The possible path for improvement of device performance and integration of nanowire junctions to Si active substrates will be pointed out.

a b c

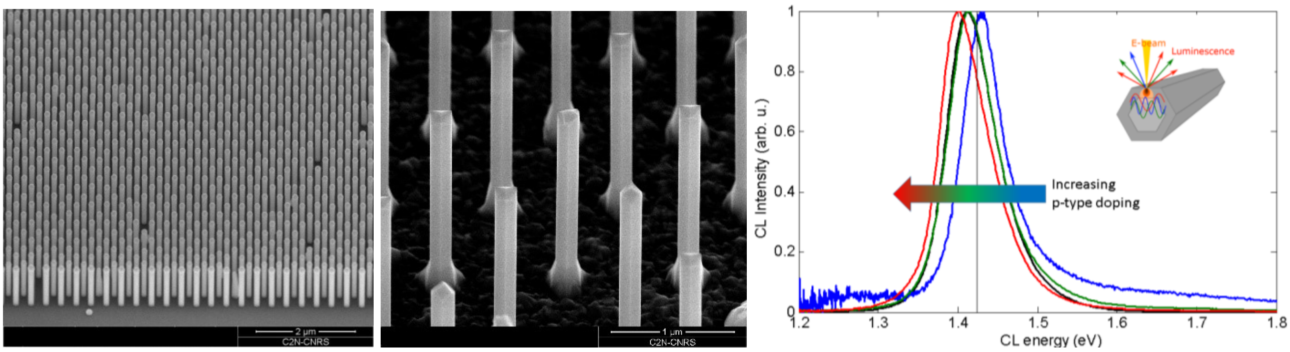

Figure (a): 45° SEM view of an array of GaAsP nanowires on Si (111), with catalyst still present at the end of the axial growth. Figure (b): 45° SEM view of GaAs nanowires with Be-doped core and AlGaAs passivation layer; the catalyst was crystallized. Figure (c): CL spectra of a series of GaAs nanowires with Be-doped shell.

[1] Grassman et al., IEEE Journal of Photovoltaics 6 (2016) 326-331
[2] Aberg et al., IEEE Journal of Photovoltaics 6 (2016) 185-190
[3] Chen et al., submitted (2017).